REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 14-20 are pending in this case. Claims 14, 15, 16, and 19 have been amended herein. Claims 14 and 19 were amended to more clearly define the claimed invention, while Claims 15 and 16 were amended to correct typographical errors.

Claims 14-20 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Arima, et al. (U.S. Patent No. 5,281,151) in view of Khandros, et al. (U.S. Patent No. 5,346,861) and Dalal, et al. (U.S. Patent Publication 2001/0013423). Applicant respectfully traverses the rejection.

Claim 14 as amended includes the feature of "applying radiant energy to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer." None of the cited references teach or suggest such a feature. For example, at paragraph [0062] Dalal states "This is done by aligning the solder interconnections with a cap of low melting point metal on the chip with the corresponding footprints on the flexible circuit carrier. The assembly is *then* held at a bias temperature . . . . [emphasis added]." Since none of the cited references teach or suggest the features of Claim 14, Applicants respectfully submits that Claim 14 is allowable over the combination of those references for at least that reason.

Claim 15 as amended includes the feature of "said wavelength causing the wafer to heat more rapidly than said interposer." None of the cited references teach or suggest such a feature. Therefore, Applicants submit that Claim 15 is patentable over the combination of those references for at least that reason.

Claim 16 as amended includes the feature of "providing an adhesive layer having first and second opposite surfaces and a multitude of electrically conductive fibers extending through electrically nonconductive material from said first surface to said second surface of the layer while remaining insulated from adjacent fibers." Arima (col. 7, lines 1-24) makes no mention of conductive fibers. None of the references teach or suggest such a layer comprising conductive fibers. Therefore Applicants submit that Claim 16 is patentable over the combination of those references for at least that reason.

Claims 17 and 18 depend from Claims 14, 15, and 16, and are therefore patentable for at least the reasons presented above for those claims.

Claim 19 as amended includes the feature of "wherein said step of applying radiant energy to said interposer heats said interposer to a temperature in the range of 75 to 80 percent of the temperature that causes said solder balls to reach a liquid state." None of the references teach or suggest such a feature. Therefore, Applicants respectfully submit that Claim 19 is patentable over the combination of those references for at least that reason.

Claim 20 includes the feature of "preheating said interposer prior to alignment with the wafer." None of the references teach or suggest such a feature. Therefore, Applicants respectfully submit that Claim 20 is patentable over the combination of those references for at least that reason.

In addition, the latest Office Action included the statement "[t]he temperature of the interposer would inherently be separately controlled in such a process because the infrared heat source would be applied only to the chip side of the structure." Applicants disagree with this reasoning. Just because the temperature is different on one side of the structure does not imply that it is separately controlled.

Finally, the last paragraph of the Office Action reads as follows: "[w]ith respect to claims 19 and 20, it would have been obvious to previously heat the interposer and allow it to cool down prior to 'alignment' or to previously cool the

interposer requiring heating prior to "alignment" because the additional steps would merely add complexity to the process without providing any advantages or solving any disclosed problems." Applicants disagree with the Examiner's statements. Applicants respectfully refer the Examiner to page 14, 2nd paragraph of the instant specification, where it is stated that "[t]his preheater raises the temperature of the film to a temperature closer to the final process temperature prior to the alignment of the film to the wafer *so that the majority of the film's thermal growth can take place prior to mating of the two surfaces* [emphasis added]." The advantage of heating the film is therefore clearly set forth in the specification. See also the first paragraph on page 15 of the instant specification for further statements as to the advantage of pre-heating.

In view of the above, Applicants respectfully request reconsideration and allowance of Claims 14-20.

Respectfully submitted,

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Claims

14. (Twice Amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a pianar array of soider balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;

applying radiant energy to said interposer and then aligning said interposer with said solder balls so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying radiant energy to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing the solder balls to reach a liquid state;

[separately controlling the temperature of said interposer in order to minimize differences in thermal expansion];

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports; and

separating the resulting composite structure into discrete chips.

15. (Twice Amended) A method for the fabrication of a semiconductor assembly comprising:

providing a silicon semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

forming a first planar array of solder balls attached to said contact pads of said plurality of chips on said semiconductor wafer so that each of said contact pads is contacted by one of said solder balls;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;

aligning said interposer with said solder ball so that each port is placed into alignment with one of said solder balls on said semiconductor wafer;

contacting said ports and said solder balls;

applying radiant energy having a wavelength of 0.8 to 2.8 μm to said semiconductor wafer such that said wafer increases uniformly in temperature and transfers heat to said solder balls, causing said solder balls to reach a liquid state;

said wavelength causing the wafer [water] to heat more rapidly than said interposer;

removing said energy such that said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

forming a second planar array of solder balls attached to said exit ports of said interposer so that each of said exit ports is contacted by one of said solder balls; and

separating the resulting composite structure into discrete chips.

16. (Twice Amended) A method for the fabrication of a semiconductor assembly comprising:

providing a semiconductor wafer comprising a plurality of undivided integrated circuit chips, each circuit chip having a plurality of metal contact pads as electrical entry and exit ports;

providing an adhesive layer having first and second opposite surfaces and a multitude of electrically conductive fibers extending through electrically nonconductive material from said first surface to said second surface of the layer while remaining insulated from adjacent fibers;

providing an interposer of electrically insulating material having first and second opposite surfaces and electrically conductive paths from said first surface to said second surface, forming electrical entry and exit ports on said insulating interposer;

placing said interposer vertically and in contact with said adhesive substrate;

providing a polymer film having a plurality of discrete adhesive areas;

providing a plurality of solder balls, one of said solder balls being placed on each of said adhesive areas;

aligning said polymer film to said interposer so that each of said solder balls is placed into alignment with one of said ports;

placing said solder balls in contact with said ports;

applying radiant energy to said semiconductor wafer such that said wafer uniformly increases in temperature and transfers [transfer] heat to said adhesive substrate, said interposer and said solder balls, causing said solder balls to reach a liquid state;

separately controlling the temperature of said interposer in order to minimize differences in thermal expansion;

removing said energy such that all said contacts form physical bonds and said solder balls cool and harden, forming physical bonds between said solder balls and said ports;

removing said polymer film; and

separating the resulting composite structure into discrete chips.

19. (amended) A method as in claim 14, wherein said step of applying radiant energy to said interposer heats said interposer to a temperature in the range of 75 to 80 percent of the temperature that causes said solder balls to reach a liquid state [further including the step of preheating said interposer prior to alignment with the wafer].